REMARKS

Claims 1-7 are all the claims pending in the application.

Claim Rejections - 35 U.S.C. § 103

Claims 1-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cabler (5,625,357) in view of Ledzius et al (5,323,157). Applicants respectfully traverse this rejection.

Claim 1 is directed to an output filter for a delta sigma modulator. With reference to the exemplary embodiment of Fig. 1, the claimed filter comprises (1) a constant current source [8a, 8b]and (2) an FIR filter [4]. The FIR filter recited in the claim has (a) a plurality of delay elements [F_1-Fn]arranged in cascade where (b) each element is operative to output data from the delta sigma modulator [2] by controlling currents from the constant current source on the basis of each of the output data. As a result, a plurality of weighted currents, that are weighted according to a filter characteristic, are generated. The weighted currents are added and outputted in an output side of the FIR filter.

Claim 2 depends from claim 1 and adds a current-to-voltage conversion unit [6] that is coupled to the output of the FIR filter and comprises a full differential operational amplifier [6a] and feedback resistors [6b].

Claim 3 depends from claim 2 and adds a single differential conversion operational amplifier [5] on the output side of the full differential operational amplifier [6].

Claim 5 depends from claim 1 and specifies that each delay element comprises a flip-flop and a respective pair of MOS transistors [F_1-F_n ;T_1 T_1*-T_n T_n*].

Claim 6 depends from claim 5 and specifies that the flip-flop generates two outputs coupled to a gate of the respective one of the MOS transistors in each pair.

Claim 7 depends from claim 1 and specifies that the current source comprises a common source for generating the plurality of weighted currents.

Cabler

The Examiner refers to Fig. 2 of Cabler for a semi-digital FIR filter current steering circuit 10, as explained at col. 3, line 28 - col. 4, line 30. The basic function of such FIR filter (otherwise referenced as a semi-digital reconstruction filter) is described with regard to the prior art circuit illustrated in Fig. 1, at col. 1, line 38 - col. 2, line 12, where application to sigma-delta D/A converters is explained (see col. 2, lines 4-13).

In Fig. 2 of Cabler, a single constant current source I_{REF} is coupled to a common conductor that supplies separate resistors R_0 R_1, each being coupled to a respective pair of switches. The switches comprise a non-inverted current switch (B_0 B_1) coupled to a non-inverted current summing node 62, and inverted current switches (B_0*, B_1*) coupled to inverted current summing node 58. Switches in each pair B_0 B_0* are controlled by the logic level of output tap B_0 of shift register 14 in Fig. 1. Similarly, switches in each pair B_1 B_1* are controlled by the logic level of output tap B_1, as explained with regard to Figs. 1 and 2 at col. 3, lines 5-37.

As explained at col. 3, lines 37-48, in order for the individual current through the resistance paths 21, 23 to remain constant, the current summing node 62, 58 must be held at identical voltages. As explained at col. 4, lines 57-60, each combination of switches B_0 and B_1 provide a value of inverting current to summing node 58 that is equal to negative value of non-inverted current provided to summing node 62.

Figure 4 is referenced by the Examiner for a teaching of a differential current being converted to a differential voltage via operational amplifier circuits 20 and 22. The circuit includes an op amp 25 and feedback resistor 30.

Ledzius et al

The Examiner admits that Cabler does not specifically teach a plurality of flip-flops connected to MOS transistors forming delay elements as part of a delta-sigma modulator or a digital signal processor. The Examiner refers to Ledzius et al for a teaching in Fig. 3 of a sigma-delta DAC including a plurality of flip-flops 81-83 that are used as delay elements where each flip-flop has two outputs each output coupled to a respective one (Fig. 4); col. 6, lines 16-40 of

the MOS transistors. The Examiner concludes it would have been obvious to one of ordinary skill to incorporate the teachings of Ledzius into the system of Cabler to improve system performance and reliability because it would improve signal to noise ratio and reduce complexity (col. 2, lines 3-5). The Examiner further concludes it would have been obvious to include such a filter apparatus and a digital signal processor or delta-sigma modulator or any other data converter where a filter is needed.

Solely to advance prosecution of particular embodiments of the present invention, Applicants have amended claim 1 to more clearly define that the constant current source as recited has first and second outputs. Claim 2 has been amended to further define that the differential operational amplifier has a pair of inputs, each input coupled to a respective one of each separate output of said FIR filter and having an output side.

In the present invention, two constant current courses (8a 8b) are used in the disclosed filter. Each of the constant current sources is connected respectively to a common output line for the inverted and non-inverted outputs of the MOS transistors. Each of the constant current sources is coupled to a separate input to the differential full amplifier 6a. The two constant current sources are used to form the differential full amplifier, which is effective to remove common mode noises peculiar to the differential. As an additional distinction, the flip-flops are connected to one another in multi-stage to form the FIR filter, which removes high-frequency components, thereby reducing noise.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Amendment Under 37 C.F.R. § 1.111
U.S. Application No. 10/730,928

Atty. Docket Q78869

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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Date: November 7, 2005